ECE 590

Digital Design using Hardware Descriptive Language

Report on
Triangular Systolic Architecture

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Introduction:

This report is to demonstrate the behavior of triangular systolic architecture (sorter) and explain each of its components and their functionality in detail. The triangular systolic architecture (sorter) works as explained.

When we give the input to the design as {X_0, X_1, X_2,..}, then we get the output as {Y_0, Y_1, Y_2,..} and the output will be sorted in the increasing order of the given input numbers.

The block diagram of the sorter is as shown below

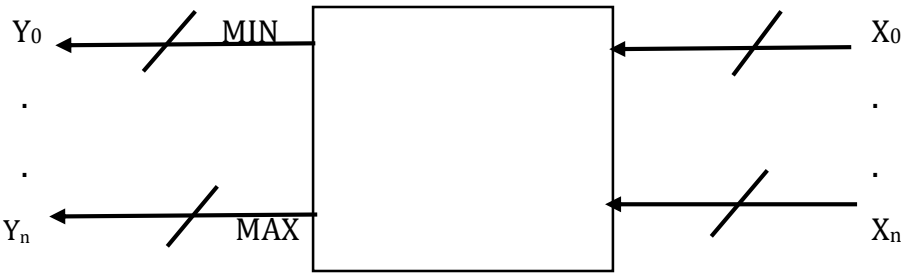


Figure: Block Diagram of a Sorter

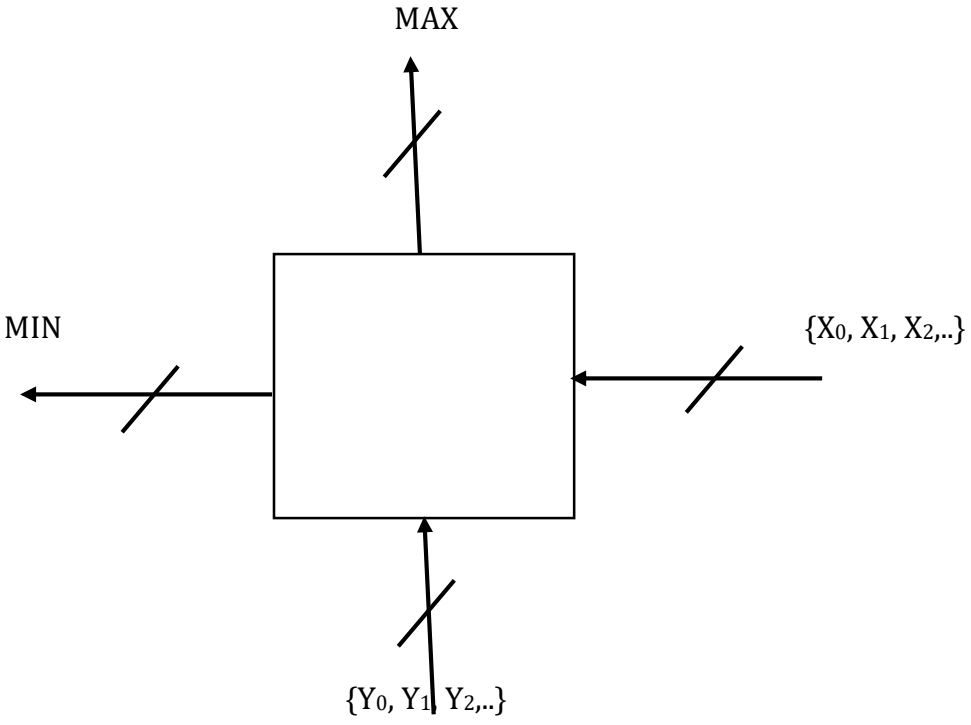


Figure: Block Diagram of a MIN/MAX Module

The MIN/MAX module is as shown in the above figure. We give the output that are needed to be sorted from the right and the bottom of the module and we get the sorted outputs from the left and the top of the module. The output that comes from the left side is the MIN and the output that comes from the right side is the MAX.

The internal details and the behavior of the MIN/MAX module is as shown in the figure below.

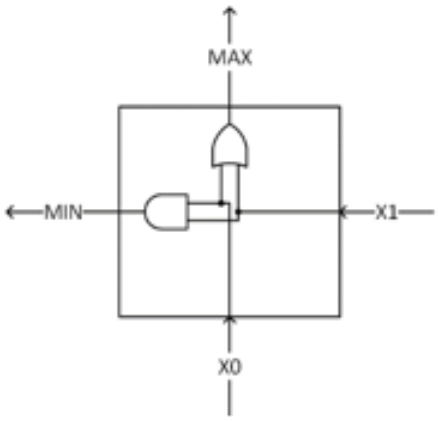


Figure: Internal Details of the MIN/MAX Module

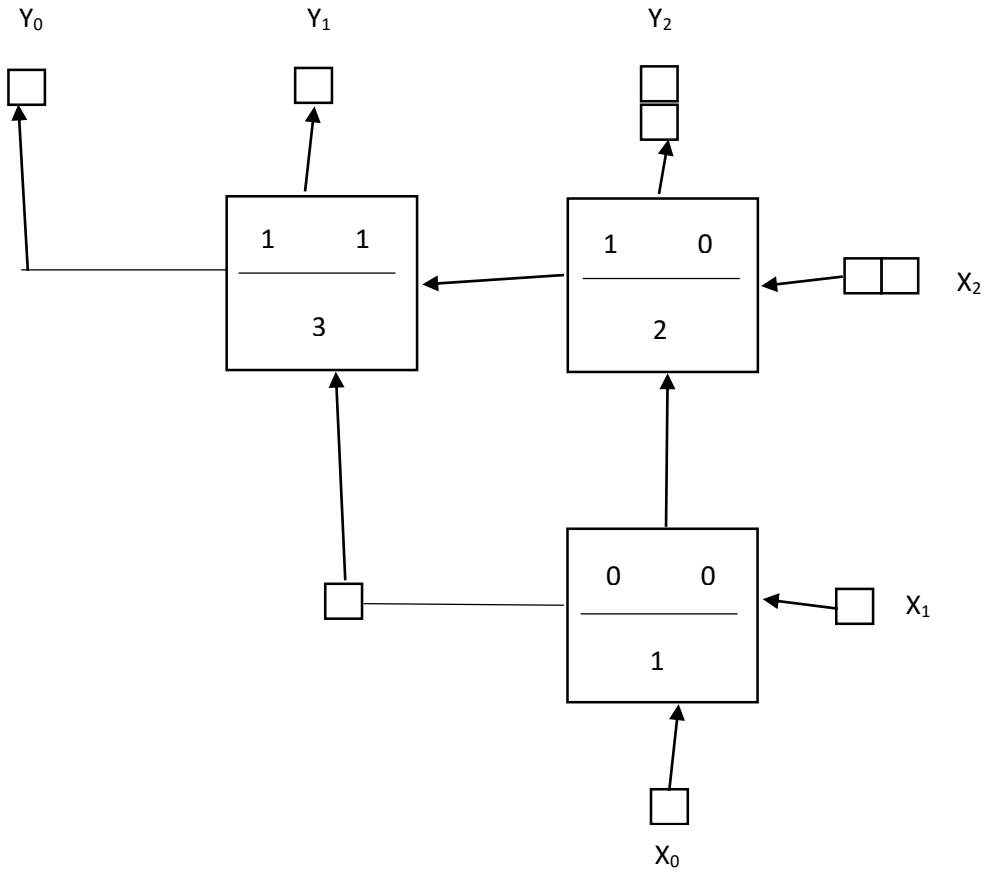
Here the inputs are X_1 and X_0. The inputs goes in through the directions shown and in the module, AND and OR operation will be performed on the inputs. The output of the AND gate will be a MAX and the output of the OR gate will be a MIN.

Here we give the input in the thermometer code fashion. Thermometer code is one of the encoding pattern in which the unsigned integer, n, is represented by n ones and the remaining zeros until the desired vector width.

For example, if our unsigned integer is 7, it is encoded in 16 bit width as 0000000001111111.

Sorter:

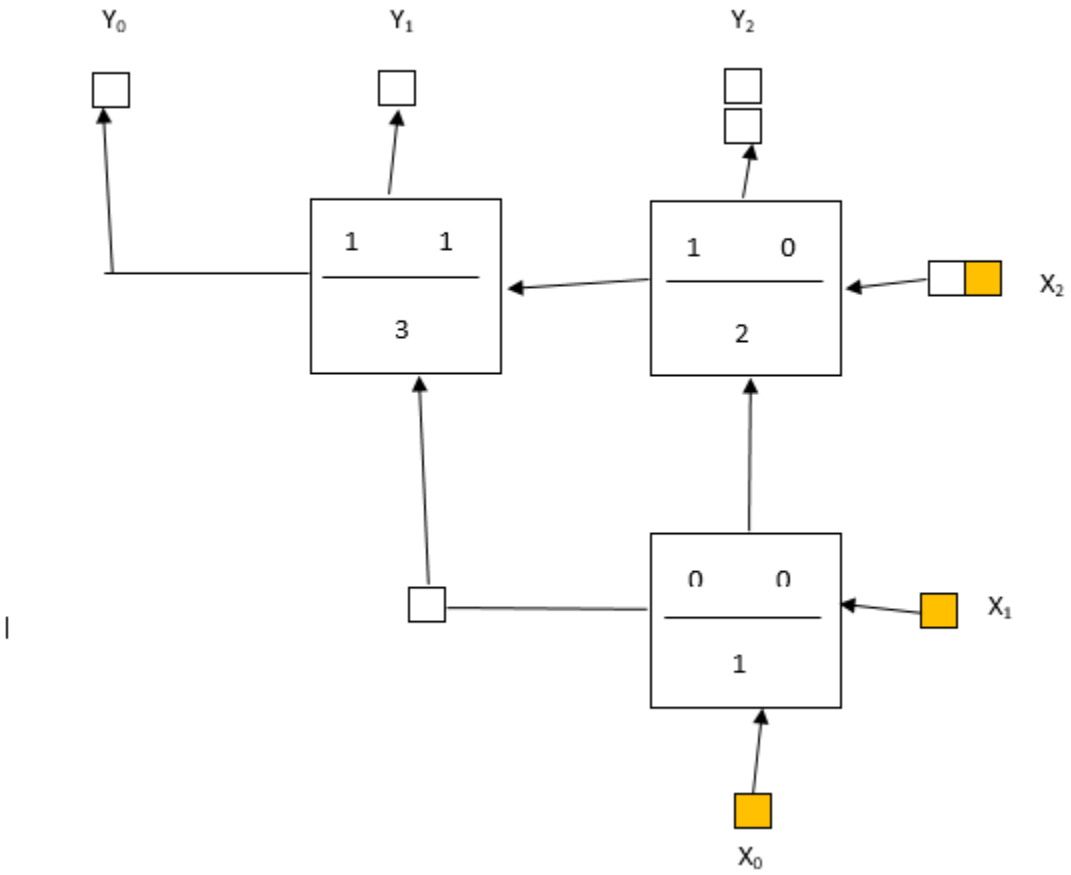
The data flow of the sorter is as shown in the figure.

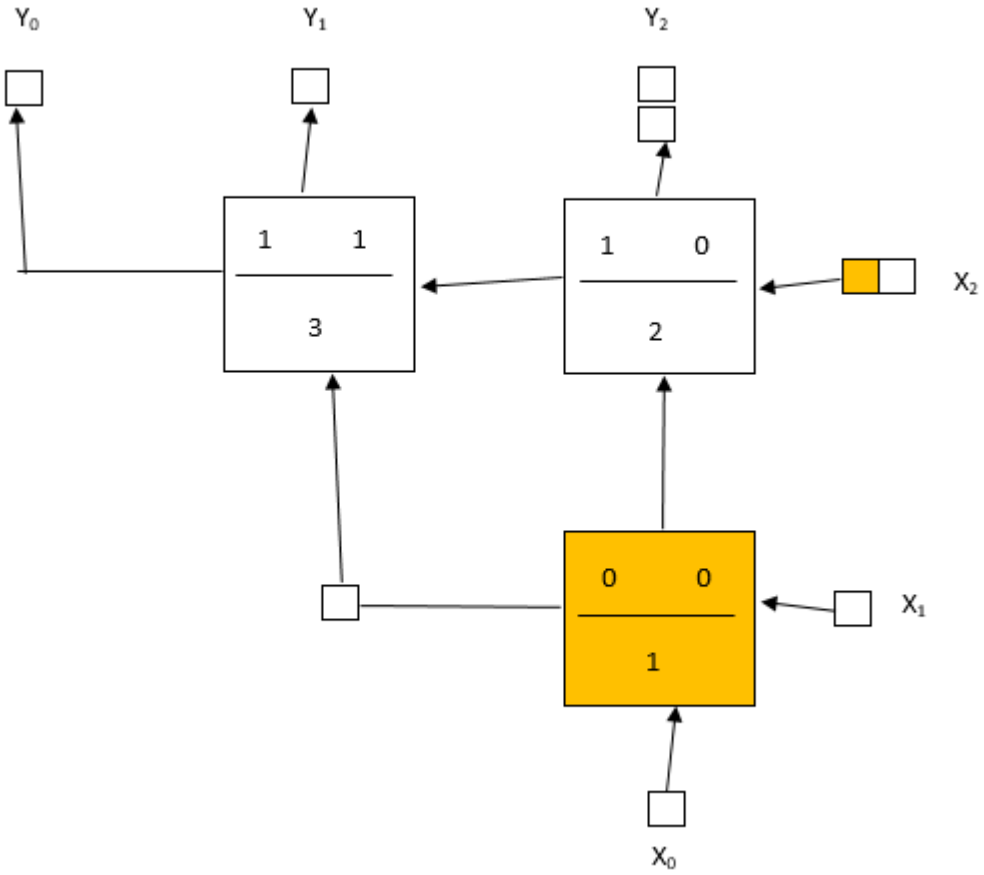


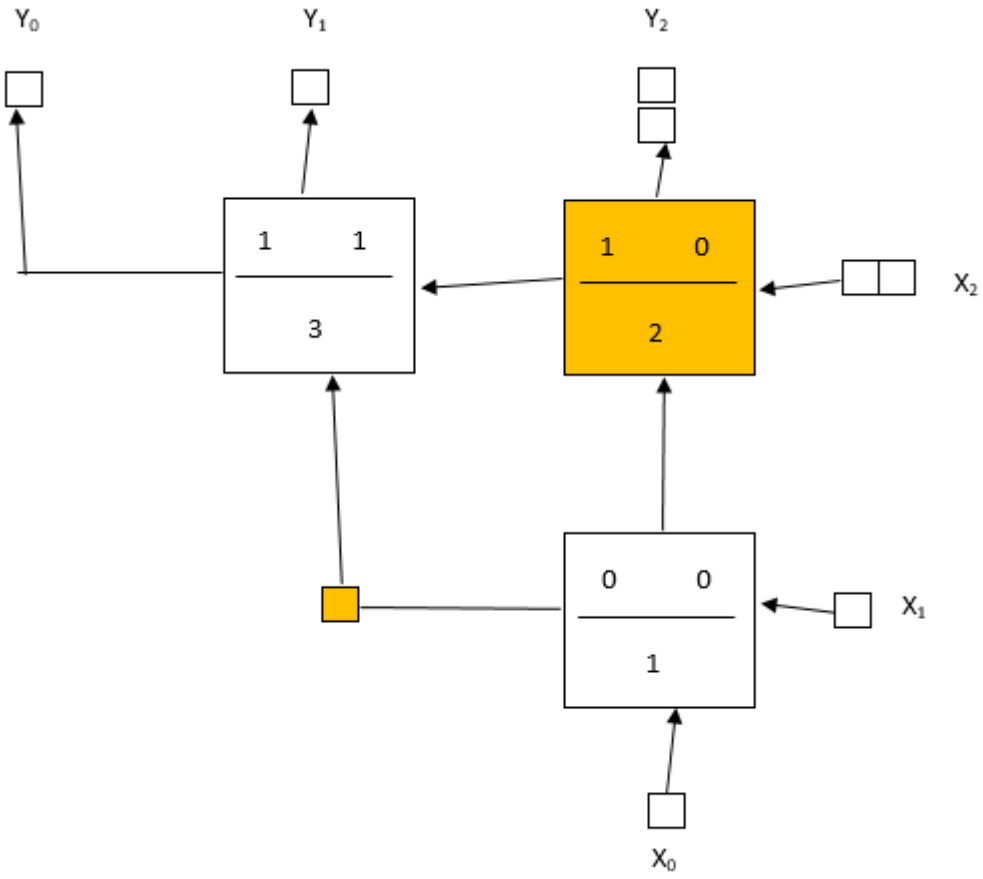
The inputs are passed here from the right as X_0, X_1, and X_2. The inputs X_0, X_1 goes through the 1st MIN/MAX module, sorted out and comes as an output. The MAX will be sent to the upper level (2,1) and the MIN will be sent to the MIN/MAX module of second level (2,2) and again the another input comes from outside. All the numbers are sorted and the output is given in the increasing format.

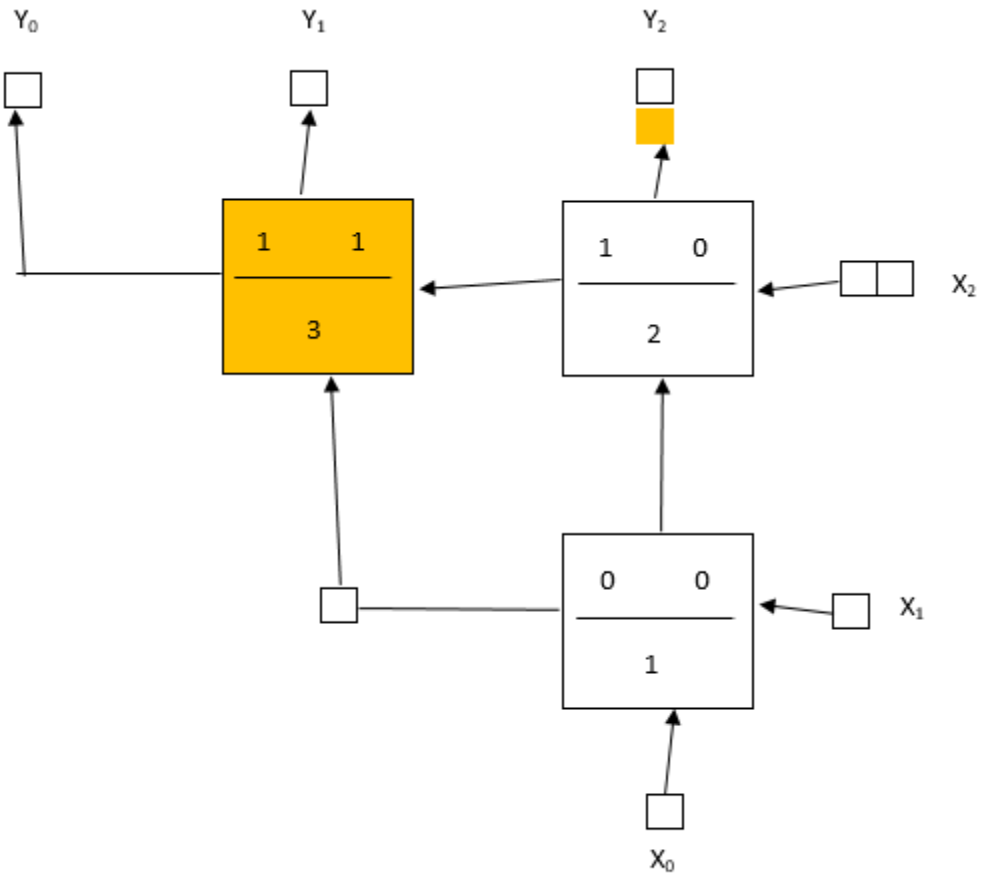
Here the MIN/MAX module is labelled with row, col and latency which means the row and col in the block indicates the Row and Column of the MIN/MAX module and the latency indicates when the MIN/MAX outputs are validated i.e., after how many cycles the outputs are validated.

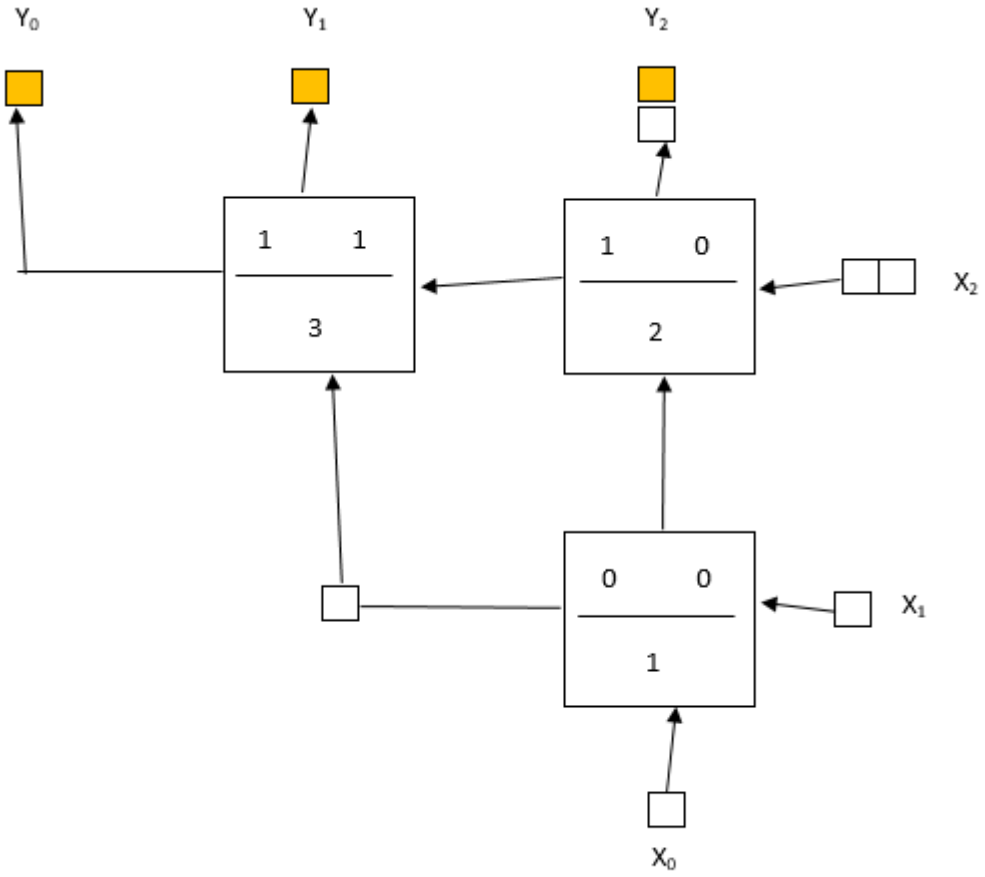
The operation of a triangular sorter is as shown.




Y0
Y1
Y2
1
1
3
1
0
2
X2
0
0
1
X1
X0


Y0
Y1
Y2
1
1
3
1
0
2
X2
0
0
1
X1
X0

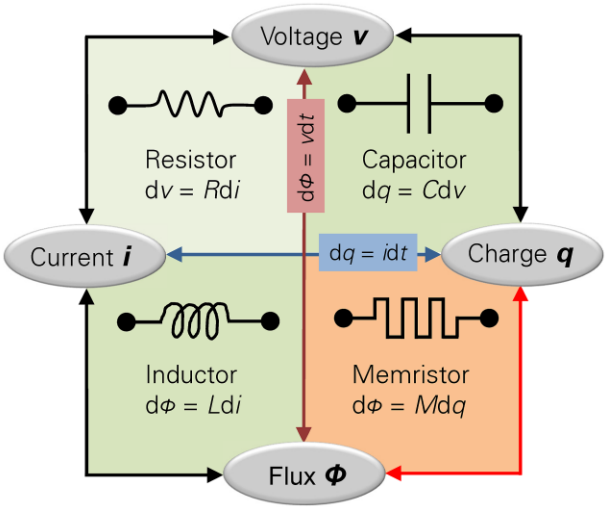

Y0
Y1
Y2
1 1
3
1 0
2
X2
0 0
1
X1
X0



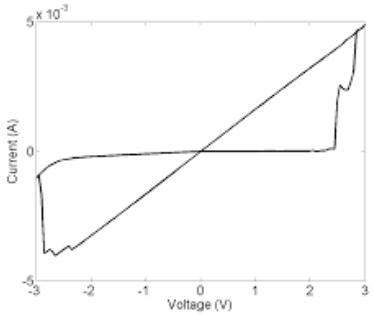
MIN/MAX Module using Memristor:

Memristor:

Memristors are the circuit elements which are similar to resistor but they have a memory. It functions same as resistor, regulates the current flow and also remembers the amount of current or the charge that flowed through it. Also, Memristors are non-volatile in nature. Hence, it is called as a Memristor – Memory Resistor. Memristor is the fourth class component along with resistor, capacitor and inductor. It is beneficial to create any circuits using memristor logic because memristor contains less number of components when compared to any other.



The I-V curve for the Memristors is as shown



Now we will design a MIN/MAX module using a memristor logic in Verilog.

```
`timescale 1ps/1ns
Module memristor #(
        Parameter N=5)
    (
        input [N-1:0] neg_input,
        input [N-1:0] mem_input,
        output [N-1:0] mem_output
    );
assign mem_output = (~neg_input) | mem_input;
end module
```

Here for the triangular systolic architecture, our group needs to do 4 modules

1. CMOS serial implementation
2. CMOS parallel implementation
3. Memristor serial implementation
4. Memristor parallel implementation

Serial implementation is as explained above and when coming to parallel implementation, we need to repeat one MIN/MAX module four times to create as one cell and continue the process.